Claims

[c1] 1. A liquid crystal display, comprising:
liquid crystal cells forming an image display area on a substrate; and
a driver for applying a voltage to said liquid crystal cells based on a reference voltage for gamma correction corresponding to digital input data, wherein said driver keeps a number of switching times for pulse strings per time unit constant for a predetermined range of said digital input data when generating the pulse strings with pulse densities corresponding to said digital input data.

[c2] 2. The liquid crystal display according to claim 1, wherein said driver is mounted on said substrate and is comprised of a plurality of driver ICs connected via signal lines.

[c3] 3. The liquid crystal display according to claim 1, wherein said predetermined range of said digital input data is a predetermined range around a medium value of said digital input data.

[c4] 4. A liquid crystal display, comprising:
liquid crystal cells forming an image display area on a substrate; and
a driver for applying a voltage to said liquid crystal cells based on a reference voltage for gamma correction corresponding to digital input data, wherein said driver has no local peak in a number of switching times for pulse strings per time unit when generating the pulse strings with pulse densities corresponding to said digital input data.

[c5] 5. A liquid crystal display, comprising:
liquid crystal cells forming an image display area on a substrate; and
a driver for applying a voltage to said liquid crystal cells based on a reference voltage for gamma correction corresponding to digital input data, wherein said driver obtains an output voltage using pulse density modulation (PDM) as well as obtains an output voltage using pulse width modulation (PWM) for a predetermined range of said digital input data around a medium value when generating pulse strings corresponding to said digital input data.

[c6] 6. A liquid crystal display driver for applying a voltage to liquid crystal cells

forming an image display area, comprising:

a pulse generation circuit for generating a plurality of reference pulses in which pulse generation densities are weighted; and

a pulse select/synthesis circuit for generating a pulse string by selecting and synthesizing necessary reference pulses on the basis of digital input data and said reference pulses, wherein said pulse generation circuit generates said reference pulses without changing a number of switching times per time unit for a predetermined range of said digital input data around a medium value.

[c7] 7. The liquid crystal display driver according to claim 6, further comprising an integration circuit for integrating the pulse string generated by said pulse select/synthesis circuit to output a voltage for gamma correction.

[c8] 8. The liquid crystal display driver according to claim 7, wherein said pulse select/synthesis circuit outputs a logical sum between a carry output from an adder circuit, which has as its inputs high order W bits of the digital input data of n bits and low order W bits of a binary counter, and a logical product between outputs X(m-1) through X(0) of said pulse generation circuit where m=n-W and the digital input data D(m-1) through D(0).

[c9] 9. The liquid crystal display driver according to claim 7, assuming that said digital input data is n bits, wherein said pulse generation circuit outputs the reference pulses using an n-bit binary counter, an n-1 bit latch, and n-1 2-input gates.

[c10] 10. A reference pulse generation circuit for generating reference pulses corresponding to n-bit digital input data, comprising:

an n-bit binary counter for counting up in synchronization with an input clock;

an n-1 bit latch for generating signals by delaying high order n-1 bits output B (n-1) through B(1) from said binary counter by one input clock period; and

n-1 logical circuits for performing logical operations with receiving as inputs said high order n-1 bits output B(n-1) through B(1) from said binary counter and the delayed signals corresponding to the high order n-1 bits output B(n-1) through B(1) from said n-1 bit latch and obtaining outputs X(0) through X(n-2) with lower reference pulse densities, whereas output X(n-1) is obtained

bypassing the logical circuit.

[c11] 11. The reference pulse generation circuit according to claim 10, wherein said n-1 logical circuits are n-1 AND circuits.

[c12] 12. The reference pulse generation circuit according to claim 10, wherein said n-1 logical circuits are n-2 AND circuits outputting X(0) through X(n-3) and a NOR circuit outputting X(n-2).

[c13] 13. A reference pulse generation circuit for digital-analog conversion employing a pulse density modulation scheme, comprising:
means for generating reference pulses that are exclusively in a high state corresponding to digital input data; and
means for generating the reference pulses such that a number of switching times for pulse strings per time unit is constant for a predetermined range of said digital input data around a medium value.

[c14] 14. The reference pulse generation circuit according to claim 13, wherein the reference pulses are generated with the frequency thereof being kept constant for half the whole range of said digital input data.

[c15] 15. A method for generating reference pulses in a digital-analog converter, comprising the steps of:
generating pulse strings with pulse densities corresponding to digital input data that is input to said digital-analog converter; and
keeping a number of switching times for said pulse strings per time unit constant for a predetermined range of said digital input data around a medium value.

[c16] 16. The method according to claim 15, further comprises the step of reducing a maximum frequency of said pulse strings to less than half of that in the case where the number of switching times is not kept constant.

[c17] 17. A method for providing an analog voltage output corresponding to digital input data, comprising the steps of:
for a range of said digital input data excluding a predetermined range around a

medium value, integrating a pulse string, whose number of pulses is adjusted depending on said digital input data, to output an analog voltage; and
for the predetermined range of said digital input data around said medium value, integrating a pulse string, whose duty is adjusted depending on said digital input data, to output an analog voltage.

[c18] 18. The method according to claim 17, further comprises the step of using the output analog voltage for a reference voltage for gamma correction in a source driver of a liquid crystal display.